However, nowhere does Adachi explicitly disclose all of the features of the independent claims, and in particular, claim 21.

Applicant notes that Adachi may disclose some sort of comparison process, which would appear to be necessary in order to ascertain the memory state of the memory cells. However, Adachi does not disclose the precise method of the comparison recited in, for example, claim 21. On this ground alone, Adachi cannot anticipate at least claim 21.

Furthermore, Adachi fails to render obvious the presently claimed invention. In fact, Adachi teaches away from the precise comparison arrangement recited in the claims. See Fig. 9 of Adachi; page 10, lines 15-18 of Adachi; and page 16, last paragraph to page 18, line 12 of Adachi. Here, it is clearly evident that Adachi teaches away from the presently claimed invention.

More specifically, with reference to page 10, lines 15-16 of the English translation of Adachi, it is stated that "voltage generated in the memory cells constructing the ferro-electric body matrix is detected by a detection circuit 45." Page 17, lines 6-9 of Adachi states that "these memory cells [in the ferro-electric layer] of same address are selected by an address decoder connected to each layer, an output from these cells is input into a sense amplifier and its output polarity is detected by a detection circuit ...". Thus, Adachi consistently discloses the sensing of the voltage across the individual memory cells in the ferro-electric ("read-out") layer and the subsequent detection, from that sensing, of the polarity of that voltage. Such sensing and detection involve reading the voltage across the memory cells, i.e., connecting the input terminals of a sensing device across the electrodes of the memory cells in the ferro-electric layer. This teaches away from the presently claimed invention in which the comparator for each row of cells is fed from the outer electrodes of the memory cells of that row. These outer electrodes are disposed on the outer faces of the two layers, not on the faces of a single, "read-out" layer, as disclosed in Adachi.

Furthermore, with reference to Fig. 9 of Adachi, it appears Adachi discloses a scheme whereby a single piezo-electric layer 51 is provided on a substrate and, disposed successively on top of that layer, a series of ferro-electric layers 53, with insulating films 52 therebetween and orthogonally disposed electrodes on the two sides of each layer. A reading voltage is applied to piezo-electric layer 51 and the memory states of the memory cells in the ferro-electric layers are detected. More precisely, cells 60 in the piezo-electric layer are selected, as required, by a suitable addressing scheme for the application of the reading voltage and the memory states on individual cells 611, 612, 613 in the ferro-electric ("read-out") layers are detected. The voltage across each memory cell is sensed and its polarity detected, as mentioned in the preceding paragraph.

More specifically, the "dummy" cells 531, 532, 533 as shown in respective ferro-electric layers in Fig. 9 of Adachi, are all polarized into the same direction of polarization and appear to act as references for detecting the memory states of the individual ferro-electric memory cells. See page 17, lines 20-21 of Adachi. In other words, the polarization state (memory state) of the memory cells 611 is compared with the fixed polarization state of the corresponding dummy cell 531, and likewise for the memory cells 612 and 613 in respect of dummy cells 532 and 533, respectively. This form of "comparison" is completely different from that of the presently claimed invention. In fact, the disclosure of Adachi would lead one skilled in the art away from the presently claimed invention.

In particular, one skilled in the art would recognize that any comparator that was used to carry out such a comparison as shown in Fig. 9 of Adachi would have inputs connected across the individual memory cells 611, 612 or 613, and either (a) the same comparator would then have its inputs transferred to across the relevant dummy cell and a comparison of the polarity of the comparator output voltage for these two cases compared, or (b) a further comparator would be used to detect the polarity of the signal across the dummy cell and a

comparison of polarity would be made between the outputs of the two comparators. Again, this is completely different from the presently claimed invention, in which the same comparator effectively simultaneously compares the signal across the piezo-electric reading layer with the signal across the ferro-electric memory layer in order to detect the polarity of the memory cells. This is achieved by connecting one input of the comparator to the electrode on the outer face of one of the two layers and the other input of the comparator to the electrode on the outer face of the other of the two layers. This configuration has the advantage of being far simpler than the arrangement (as implied) by Adachi, in which either two comparators must be used, or the same comparator must be disconnected from one cell (the memory cell) and connected to the dummy cell in order to detect polarity.

As a courtesy to the Examiner, and to further support Applicant's arguments presented herein, Applicant provides a marked-up version of Fig. 9 of Adachi showing scenarios (a) and (b) as discussed above. For comparison, a third figure of the presently claimed invention is also submitted.

For the foregoing reasons, Applicant submits that the presently claimed invention is not anticipated or rendered obvious by Adachi. Withdrawal of the rejection is thus respectfully requested.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Linda M. Saltiel
Registration No. 51,122

JAO:LMS/djb

Attachment:
Figures

Date: October 4, 2005

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461